WBC-HRA381-M10

Datasheet

Catalog

1. Product Overview

WBC-HRA381-M10 is a smart microphone module featuring high signal-to-noise ratio, high acoustic overload point, and an integrated ultra-low-power analog-digital hybrid AI chip that combines sensing, storage, and computing. This module incorporates a MEMS sensor, ASP intelligent voice analog preprocessing unit, and NPU processing unit, enabling ultra-low-power offline voice detection, keyword recognition, and other interactive functions.

1.1. Key Features

1.1.1. High-Performance Microphone

- Package Dimensions: 3.5 x 2.65 x 1.0mm
- Sensitivity: ±1dB
- High Signal-to-Noise Ratio: 65dBA
- High Acoustic Overload Point: 127dBSPL

1.1.2. Built-in Neural Processing Unit (NPU)

- Neural network processing: BNN/CNN processor cores
- Supports ultra-low power voice wake-up
- Supports VAD voice detection

1.1.3. Analog Signal Processing (ASP)

- LNA with 8-level configurable gain
- Automatic Gain Control
- Event-driven ultra-low power analog-to-digital conversion

1.1.4. Built-in voice detection and keyword recognition

- Built-in μW-level ultra-low power analog VAD
- KWS supports up to 30 keywords

1.1.5. Memory

- Supports 32KB OTP
- Built-in 64KB SRAM

1.1.6. Peripheral interfaces

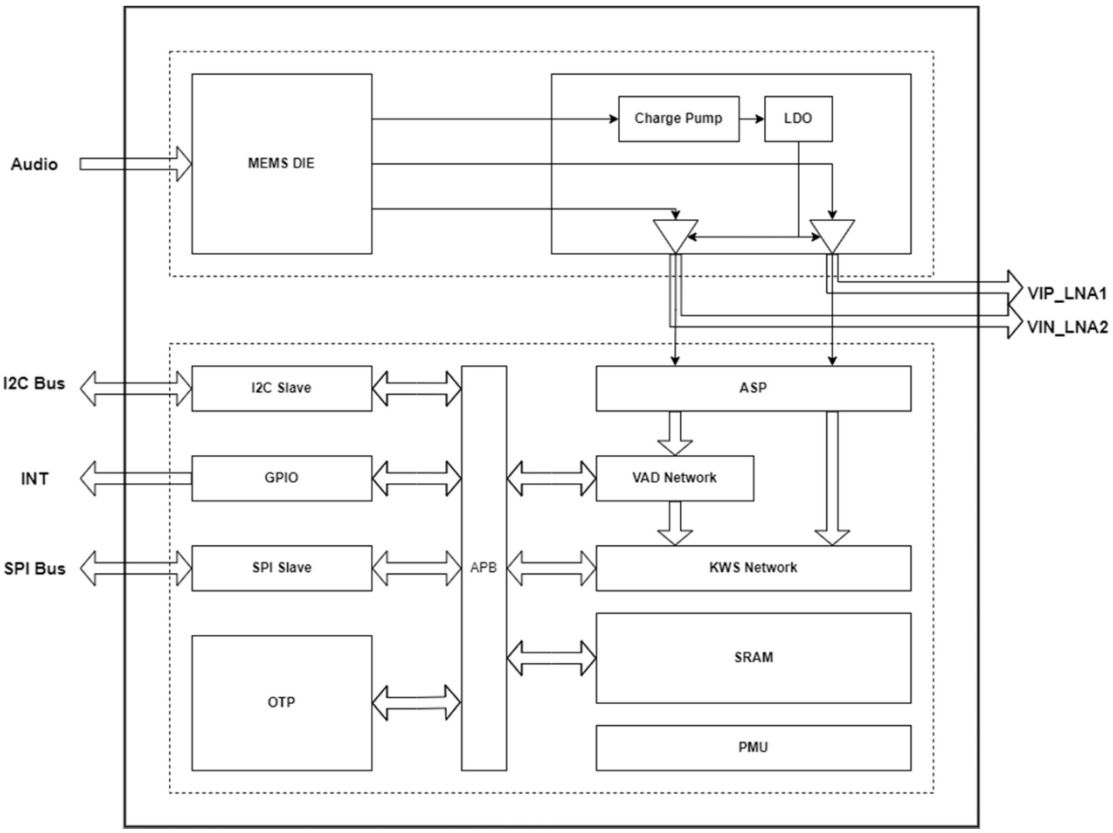
- 1 Slave I2C interface

1.1.7. Typical Applications

- TWS earbuds, smartwatches, AR/VR glasses, smartphones, smart home devices, etc.

2. Functional Description

2.1. Functional Block Diagram



2.2. Module Function Introduction

- ASP: Analog Signal Processing Unit, performs filtering and feature extraction on analog signals from the microphone.
- LP_NPU: Low-power Neural Processor. This unit employs a small binary BNN neural network to detect non-steady signals, providing binary classification outputs for the smoothness characteristics of input signals. It can be used for low-power tasks such as Voice Activity Detection (VAD) and Anomaly Event Detection (AED).The overall power consumption of LP_NPU is exceptionally low, enabling it to remain in an Always-on (AON) state. It only activates the NPU for more complex neural network classification tasks upon detecting valid voice signals or anomaly events. Simultaneously, it can trigger interrupt outputs to report events to the external master SoC.
- NPU: Neural Processor Unit. This unit consists of a deep separable CNN network that performs multi-class classification on input data. It can be widely used for tasks such as Keyword Spotting (KWS) and Scenario Classification.Upon detecting pre-trained classification outputs, the NPU triggers interrupts to report to the external master SoC. This unit defaults to sleep mode, awaiting LP_NPU wake-up signals to perform classification tasks before returning to sleep.

. After completing classification tasks, it returns to sleep mode.

- PMU: Power Management Unit. Manages low-power operation across all units and generates timing control signals during mode transitions. The PMU defaults to disabling the NPU until the LP_NPU output wakes other functions; it also disables the NPU after task completion.
- SCR: System Control Register. Performs internal circuit configuration, implements peripheral port communication, and manages internal/external interrupt functions. After power-up, the system boots from internal OTP, configures peripheral interface unit parameters, completes basic chip configuration (peripheral ports), and waits for the external master chip to configure internal LP_NPU and NPU parameters via peripheral ports.
- CRG: Clock & Reset Generator. Provides clock and reset signals to all modules.
- APB Matrix: Internal APB interconnect bus connecting the HAC, peripherals, and VAD/KWS units to enable data exchange between modules.
- I2C Interface: I2C standard interface for communication between the chip and external devices.
  - Standard two-wire mode, including data line SDA and clock line SCL.
  - Supports up to 400Kb/s
  - Supports slave mode only
  - Supports 7-bit addresses only
- Supports burst read/write operations for internal memory

3. Operating Modes

3.1. Voice Activation Detection Mode (VAD Mode)

In this mode, the chip continuously performs voice detection and recognition inference calculations. The chip's power consumption is extremely low, approximately 70uA. When the inference result indicates a voice signal, an interrupt is generated to wake up the controller or other processors. Upon receiving the interrupt, the controller or processor performs its own subsequent operations.

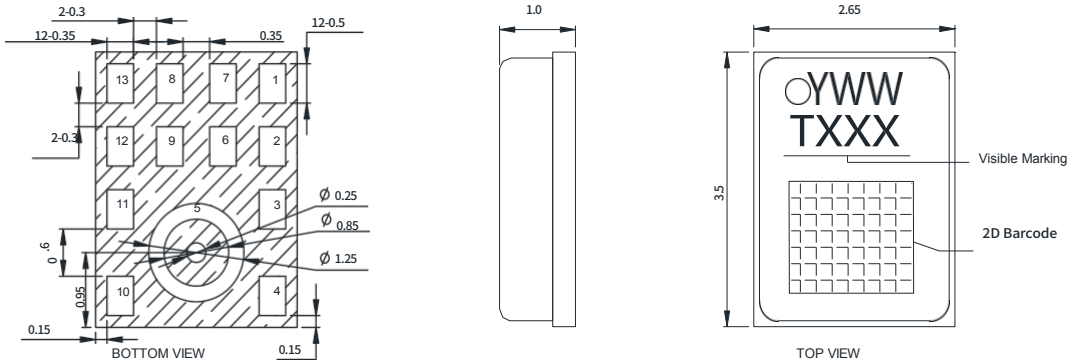
3.2. Continuous Speech Recognition Mode (KWS Mode)

In this mode, the chip continuously performs keyword recognition inference calculations with a power consumption of approximately 160uA. Upon successfully matching the inference result with the pre-trained keyword, an interrupt is generated to wake up the controller or other processor. After receiving the interrupt, the controller or processor actively reads the keyword result from the designated register via the IIC data port to execute corresponding actions.

3.3. Low-Power耗 Voice Wake-Up Mode (VAD+KWS Mode)

In this mode, the chip continuously performs voice detection and recognition inference calculations with extremely low power consumption of approximately 70μA. When the inference result indicates a human voice, an internal trigger mechanism activates, causing the chip to enter KWS mode for keyword recognition inference calculations. Finally, upon successful matching of the keyword inference result with the pre-trained data, an interrupt is generated to wake up the controller or other processor. Upon receiving the interrupt, the controller or processor actively reads the keyword result from the designated register via the IIC data port.

4. Mechanical Structure



Unit: mm Unmarked Tolerance: ± 0.1 (mm)

Item	Dimension	Tolerance
Length	3.5	±0.1
Width	2.65	±0.1
Height	1.0	±0.1
Acoustic Port	0.25	±0.05

No	PIN Name	Direction	Description
1	VCC	P	Processor Analog Power Supply
2	VDD	V	Microphone Power Supply
3	PAD_VADINT	DO	VAD Wake-up Interrupt Output
4	AGND	G	Analog Ground
5	GND	G	Microphone Ground
6	PAD_KWSINT	DO	KWS Wake-up Interrupt Output
7	VIP_LNA1	AOUT	Analog Microphone Signal Output Terminal
8	PAD_RSTN	DI	Processor Hardware Reset Port
9	VDDIO	P	Processor Digital IO Power Supply
10	DGND	G	Digital Ground
11	PAD_SDA	DIO	I2C Slave Interface Data Pin
12	PAD_SCL	DI	I2C Slave Interface Clock Pin
13	DVDD09	AIO	Digital Core Power Supply

5. Electrical Characteristics

5.1. Limit Parameters

Parameter	Min	Typ	Max	Unit
Processor-related:				
Analog Power Supply	-0.3		3.6	V
Digital IO Power Supply	-0.3		3.6	V
VIP_LNA1	-0.3		3.6	V
Other Input/Output	-0.3		3.6	V
Microphone-related:				
Power Supply			4.2	V
System and Packaging Specifications:				
Operating Temperature Range	-40		85	℃
Storage Temperature Range	-40		100	℃
ESD (HBM)	-2000		2000	V

5.2. Performance Specifications

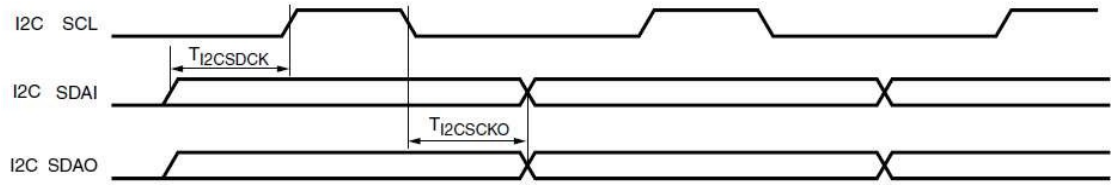
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Processor-related:						
Power Supply	VCC		1.6	3.3	3.6	V
	VDDIO		1.6	3.3	3.6	V
	DVDD09			0.9		V
System Clock				6.144	12.288	MHz
Standby Power Consumption		VAD active, KWS in sleep mode State		70		μA
Active state		VAD and KWS are both active		170		μA
VAD detection delay Time		Signal from analog microphone to the VAD unit to the VAD output interrupt		10		ms
KWS detection delay time		Time from speech end to KWS unit output interrupt		8		ms
Microphone-related:						
Power Supply	VDD		1.6	2.0	3.6	V
Sensitivity	S	f=1kHz, Pin=1Pa, 0 dB = 1 V/Pa	-39	-38	-37	dB
Directionality			Omnidirectional			
Polarity		Sound Pressure Variation Characteristics	Increase in Output Voltage			
Sensitivity vs. Voltage	ΔS	Vs=3.6V~1.6V		<0.5		dB

Voltage				

Output impedance	Zout	f=1kHz			400	Ω
Current Power Consumption	I	1.6 V to 3.6V		125	200	μA
Signal-to-noise ratio	S/N	20-20kHz Bandwidth, A-weighted		65		dBA
Total Harmonic Distortion	THD	94dB SPL @1KHz		0.05	0.5	%
Acoustic overload point	AOP	THD 10%@1KHz		127		dBSPL
Power Supply Rejection Ratio	PSR	100mVpp Squarewave @217Hz, A-weighted		-90		dB
Power Supply Ripple Rejection Ratio	PSRR	200mVpp Sinewave @1KHz		60		dB
DC Output	VDC			0.85		V
Output Load	Cload				100	pF
	Rload		8			kΩ

5.3. I2C Digital Interface Characteristics

a. I2C Interface Timing



b. I2C Interface Specifications

	Description	Min	Typ	Max	Unit
$T_{DCI2CFCLK}$	SCL duty cycle	–	50	–	%
$T_{I2CFCKO}$	SDAO clock to output delay	–	–	900	ns
$T_{I2CFDCK}$	SDAI setup time	100	–	–	ns
$F_{I2CFCLK}$	SCL clock frequency	–	–	400	kHz

6. PCB Design and Layout Guidelines

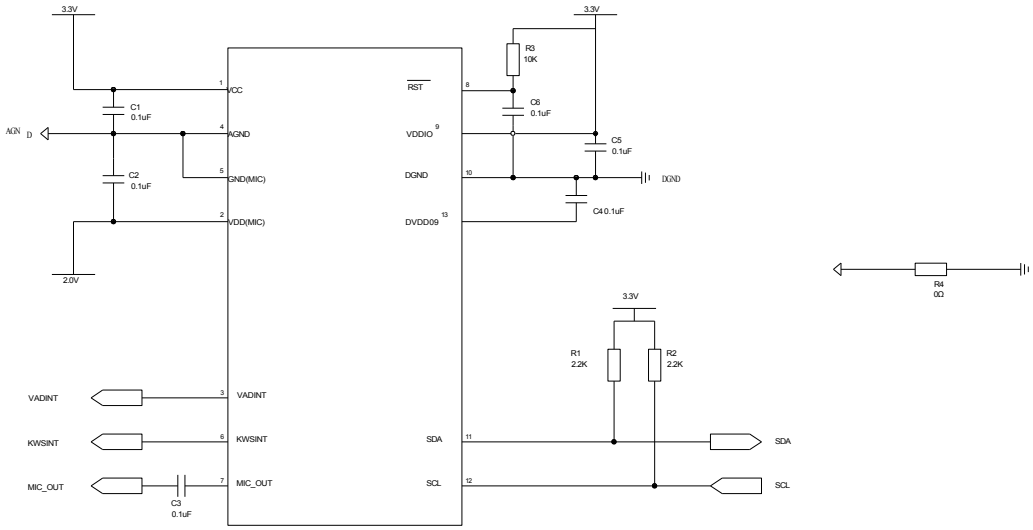
6.1. Power Planes

Power supply noise significantly impacts analog circuits. System power design requires low-impedance power planes and decoupling capacitors. Noise-sensitive power pins may additionally require decoupling capacitors (0.1µF), with traces kept as short as possible to prevent coupling additional noise into the power supply.

6.2. Signal Routing

- Keep MIC traces as short as possible. Trace routing should be grounded as much as possible, and the bottom reference ground plane should be kept as complete as possible.
- Position the MIC circuit as far as possible from interference sources (such as DC-DC chokes, crystal oscillators, and high-current networks).
- Separate analog and digital grounds, ultimately bridged with a 0-ohm resistor.
- Place power filter capacitors as close to the pins as possible.

6.3. Typical Applications



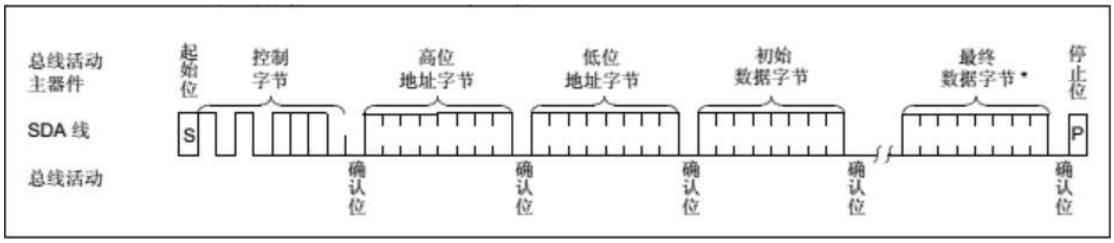
I2C Mode Application Diagram

I2C Read/Write Introduction:

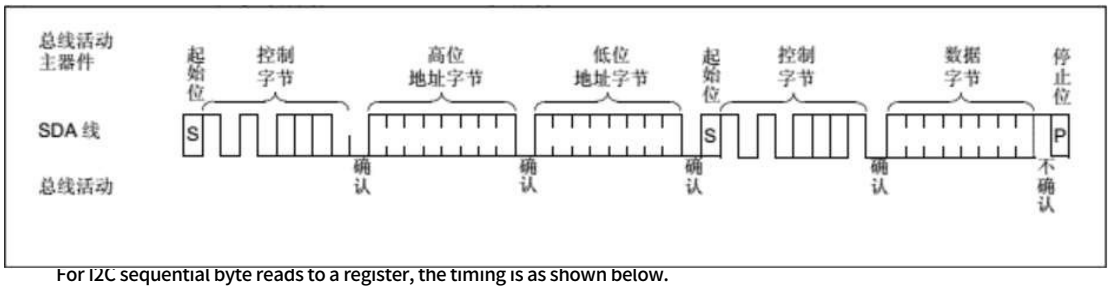
a. The chip's I2C interface slave address is a 7-bit address, which is 0x5A.

b. Per I2C protocol: - Read/Write bit R is high level - Write bit W is low level c. Address and data transmission: - High byte transmitted first - Low byte transmitted second

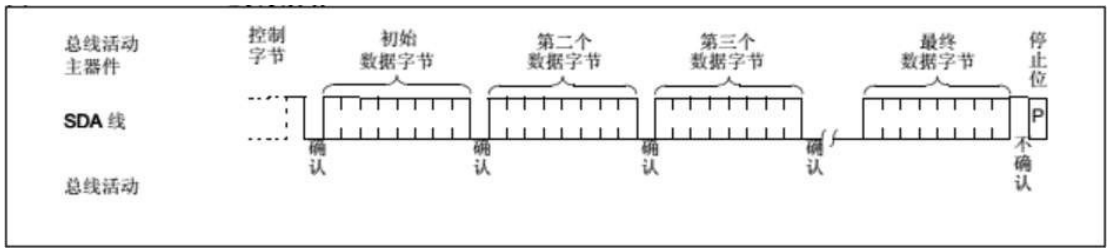
d. When sending address and data bytes, the most significant bit (MSB) is transmitted first, followed by the least significant bit (LSB). When writing to an I²C register, the timing is as shown below:



For I2C single-byte register reads, the timing is as shown below.



For I2C sequential byte reads to a register, the timing is as shown below.



7. Reliability Specifications

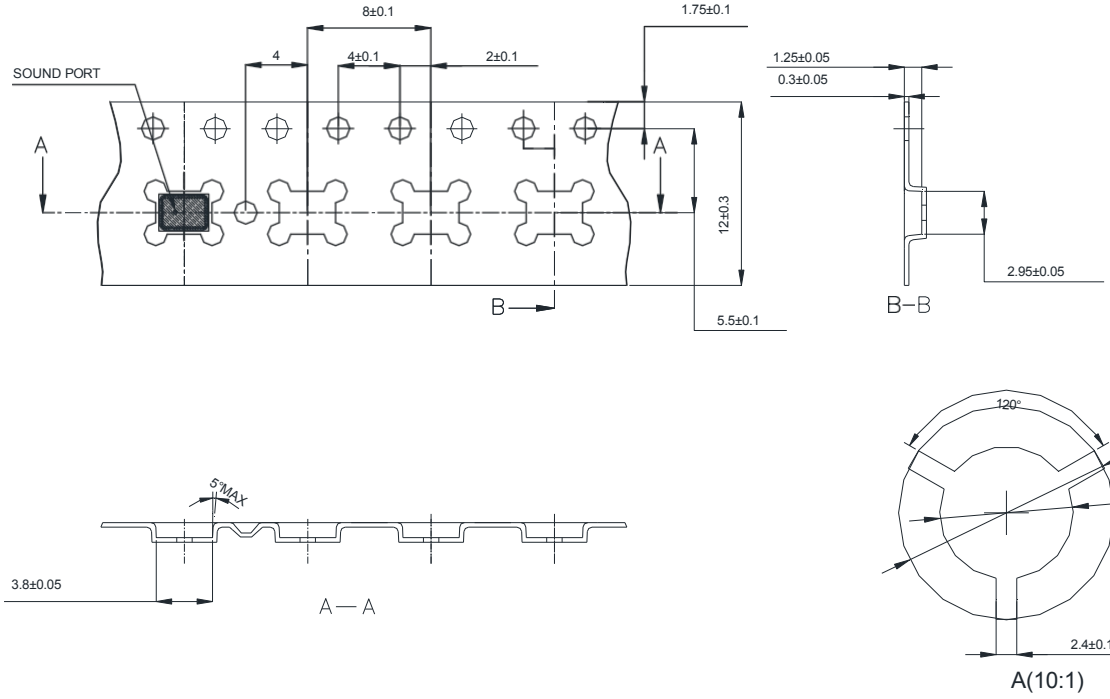
No.	Item	Test Condition
1	Pre-treatment	Baking: 125°C/24 hours, soaking at 85°C, 85% RH for 168 hours, completed Reflow soldering: 3 cycles, maximum reflow temperature 260°C.
2	High-Temperature Storage Test	105±3°C, 1000 hours, recovery 2 hours
3	High-Temperature Power-On Test	105±3°C, maximum voltage, 1000 hours, recovery 2 hours
4	Low-Temperature Storage Test	-40±3°C, 1000 hours, recovery 2 hours
5	Low-Temperature Power-Up Test	-40±3°C, maximum voltage, 1000 hours, recovery 2 hours
6	High-temperature and high-humidity power-on test 1	85±3°C, 85% RH, at maximum bias voltage, 1000 hours, recovery 2 hours, no corrosion or deformation inside the microphone after testing
7	High Temperature and Humidity Power-On Test 2	65±3°C, 95% RH, at upper limit bias voltage, 168 hours, recovery 2 hours hours. After testing, the interior of the microphone should show no corrosion or deformation.
8	Thermal Shock Test	Dual-chamber method: -40°C for 15 min → 125°C for 15 min, 100 cycles, recovery 2 hours
9	Vibration Test	X, Y, Z axes, 12 minutes per axis, frequency: 20–2000 Hz,

		peak acceleration 20g, recovery 2 hours
10	Drop Test	Height: 1.5 meters Fixture weight: 150g (Sound hole diameter in fixture ≥ 0.8mm) Reference surface: Smooth marble floor Duration: 4 corners × 4 times, 6 surfaces × 4 times Sensitivity change after testing should be less than 1 dB
11	Drum test	Height: 1.0 m Fixture weight: 150 g (Sound hole diameter in fixture ≥ 0.8 mm) Duration: 300 cycles Recommended Frequency: 10-11 cycles/min Sensitivity change after testing should be less than 1 dB
12	Electrostatic test 1	a. HMB Discharge location: I/O pins Charging voltage: ±3000V Discharge network: 100 pF & 1500 Ω b. CDM Discharge Location: I/O Pins Charging Voltage: ±250V
13	Electrostatic Test 2	Test conducted per IEC 61000-4-2 Level 3: a. Contact discharge Discharge location: MIC output terminal Charging voltage: ±6000V DC Discharge network: 150pF & 330Ω b. Air Discharge Discharge location: Sound hole Charging voltage: ±8000 V DC Discharge network: 150pF & 330Ω
14	Structural Impact Test	10,000 g, duration: 0.1 ms, X/Y/Z three directions, three times per direction; sensitivity change after test should be less than 1 dB
15	Reflow	Perform 3 reflow cycles with a peak temperature of +260°C according to the reflow profile

8. Packaging

* Use anti-static trays and tape for packaging.

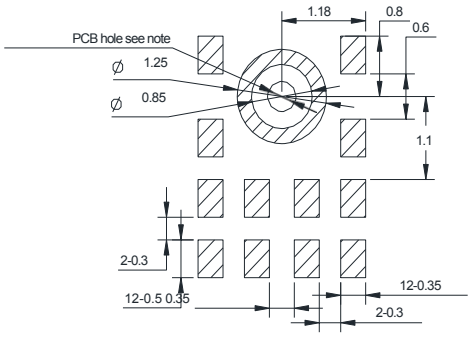
* Implement electrostatic discharge (ESD) protection measures during packaging operations.



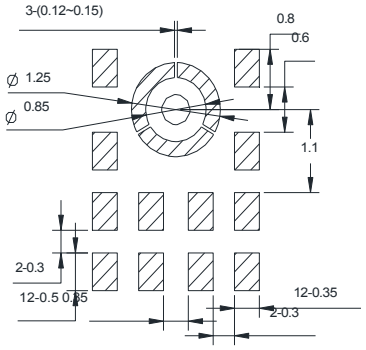
Tape and Reel	ϕ330mm	5,500PCS×1=5,500PCS
Shipping Box	215mm × 370mm × 370mm	5,500PCS×10=55,000PCS

9. Application Design Recommendations

9.1. Recommendations for Pad Design and Solder Paste Printing Board Design



Recommended PCB Pad Design



Recommended Solder Paste Printing Board Design

Note:

Unless otherwise specified, dimensions are in millimeters.

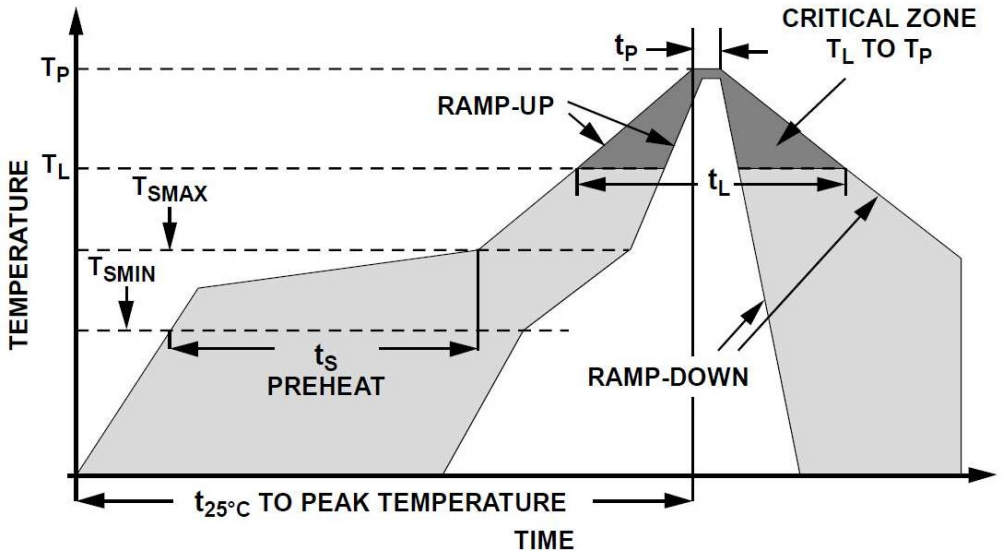
Unless otherwise specified, tolerances are ±0.1mm

Recommended PCB non-metallized hole diameter: 0.4–0.6 mm.

9.2. Reflow Temperature Profile

Temperature Distribution During Reflow Process

Parameters		Reference	Specification
Average Rate		T_L to T_P	Maximum 3°C/sec
Preheat	Minimum Temperature	T_{SMIN}	150°C
	Maximum Temperature	T_{SMAX}	200°C
	Heat-up time	t_S	60 sec t o 180 sec
Heat-up rate		T_{SMAX} to T_L	1.25°C/sec
Solder Paste Liquid Holding Time		t_L	60 sec to 150 sec
Liquefaction temperature		T_L	217°C
Peak temperature		T_P	260°C +0°C/–5°C
Time at actual peak temperature +5°C		t_P	20 sec to 40 sec
Temperature Decay Rate		T_P to T_{SMAX}	6°C/sec max
Time from +25°C to maximum temperature			8 min max



Reflow curve diagram

Additional Notes:

If multiple reflows are required, the MIC should cool to room temperature before the next reflow.

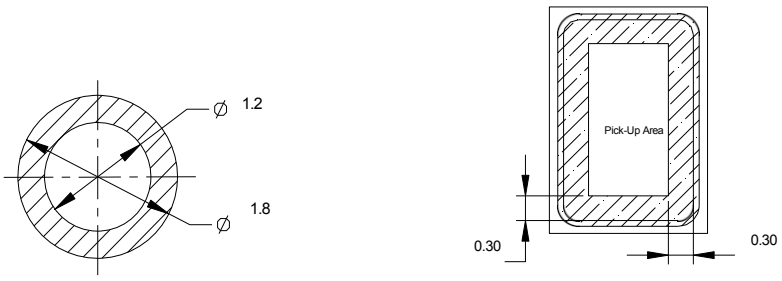
No more than 3 reflow cycles are recommended.
After reflow, do not clean the board with liquids
or ultrasonic cleaning. Do not apply vacuum
directly to the MIC's audio port.

Never insert any object into the MIC's audio port under any circumstances.
For double-sided PCBA, it is recommended to mount the MIC during the
second placement. Do not seal the audio hole during reflow.

If there is a risk of cracking, it is recommended to set the peak reflow temperature below 240°C or above 255°C.

9.3. Recommended MIC

Outer diameter:
Φ1.8mm Inner
diameter:
Φ1.2mm



Tip Size and MIC Pick-Up Area

10. Special Precautions

10.1 Air Gun Cleaning Specifications

Do not point the air gun directly at the MIC sound hole. Recommended conditions:
Air pressure < 0.3MPa;
Distance >5cm;

Duration < 5 sec.

10.2 Packaging

Do not store the MIC in a vacuum environment. Vacuum sealing may cause damage to the MIC.

10.3 Storage

Meets MSL (Moisture Sensitivity Level) 1 requirements. Store MIC in a warehouse with humidity below 75%. Do not store in areas subject to sudden temperature changes, acidic gases, any other harmful gases, or strong magnetic fields.
Protect the product from damage caused by moisture, vibration, light exposure, and external forces. Implement appropriate anti-static measures during assembly and transportation.

Use the original shipping packaging for long-term storage.

10.4 Disposal

For discarded microphones, customers must comply with the provisions of the Waste Electrical and Electronic Equipment (WEEE) Directive (2002/96/EC).

11. Version

Version	Description	Date
V1.0	Initial Release	2025-01-14
V1.1	Updated delay, current, PSR, PSRR, VDD range	May 12, 2025
V2.0	Updated company information	August 19, 2025
V3.0	Updated application circuits, AOP, and packaging drawings	November 21, 2025