XJ1801

250V 3-Phase Gate Driver
User Manual

Wuxi Silicon Source Technology Co., Ltd.

Add:555-820 Liangqing Road Wuxi, Jiangsu China

P.C. 214000

Tel : 0510-85880729

htttp :// www.sistc.com

Catalogue

Graph Catalogue

Table Catalogue

1 Description

JSC1801 is an integrated three-independent half-bridge gate driver IC designed for high voltage, high speed drive MOSFETs that operate up to +250V.

JSC1801 has a built-in VCC/VBS under-voltage protection (UVLO) function to prevent the power tube from operating at too low a voltage.

JSC1801 has built-in shoot-through prevention and dead time to prevent shoot-through of the driven high and low side MOSFET or IGBT, effectively protecting power devices.

JSC1801 has built-in input signal filtering to prevent input noise interference.

2 Key Features

- Suspension absolute voltage + 250V
- Gate driver supply range from 4.9V to 20V
- Integrated three-independent half-bridge gate driver
- Transient pulse current +0.9A/-1.35A
- 3.3V/5V logic input compatible
- VCC/VBS under-voltage protection (UVLO)
- Internal shoot-through prevention
- Internal dead time of 250 ns
- Integrated input filter function
- Outputs in phase with inputs

3 Application

Three-phase brushless DC motor drive

4 Packages

Packaging as shown in the following figure

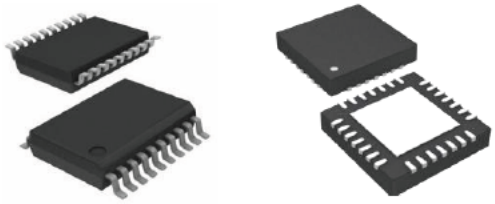


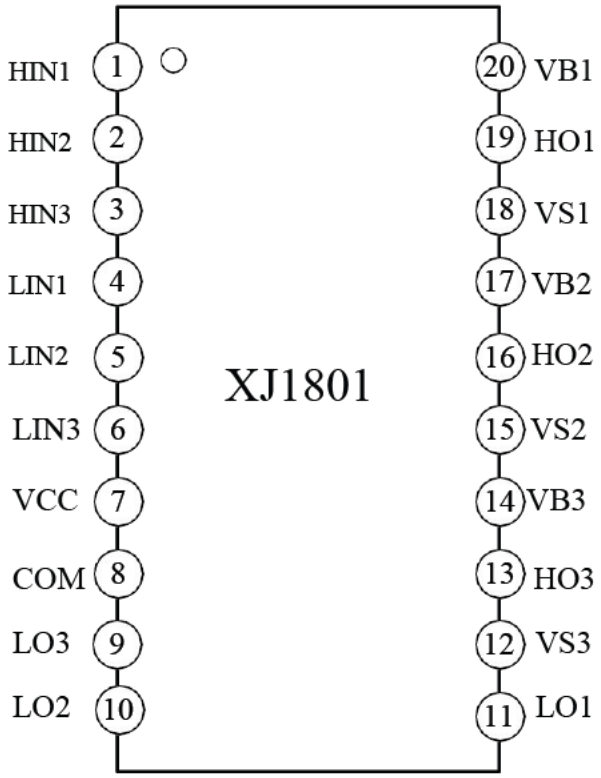
Figure. 1 Schematic representation of the chip package

Product name	Packaging forms	Model
XJ1801CTS20	TSSOP20	XJ1801CTS20
XJ1801QFN24	QFN24	XJ1801QFN24

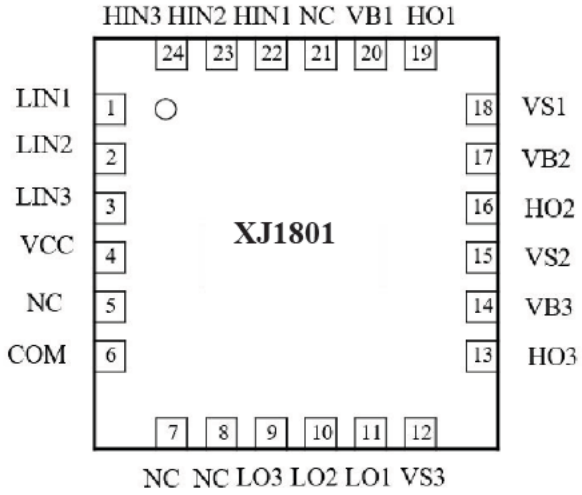
5 Lead configuration

5.1 Lead assignments

TSSOP20



QFN24



5.2 Lead definitions

TSSOP20

Number	Symbol	Description
1,2,3	HIN1,HIN2,HIN3	High side input
4,5,6	LIN1,LIN2,LIN3	Low side input
7	VCC	Low side supply
8	COM	Low side return
9,10,11	LO3,LO2,LO1	Low side gate drive output
12,15,18	VS3,VS2,VS1	High side floating supply return
13,16,19	HO3,HO2,HO1	High side gate drive output
14,17,20	VB3,VB2,VB1	High side floating supply

QFN24

Number	Symbol	Description
22,23,24	HIN1,HIN2,HIN3	High side input
1,2,3	LIN1,LIN2,LIN3	Low side input
4	VCC	Low side supply
6	COM	Low side return
9,10,11	LO3,LO2,LO1	Low side gate drive output
12,15,18	VS3,VS2,VS1	High side floating supply return
13,16,19	HO3,HO2,HO1	High side gate drive output
14,17,20	VB3,VB2,VB1	High side floating supply
5,7,8,21	NC	No connection

Table. 1 The lead definitions of the XJ1801

6 Functional block diagram and description

6.1 The functional block diagram of the JSC1801 is shown in the following figure:

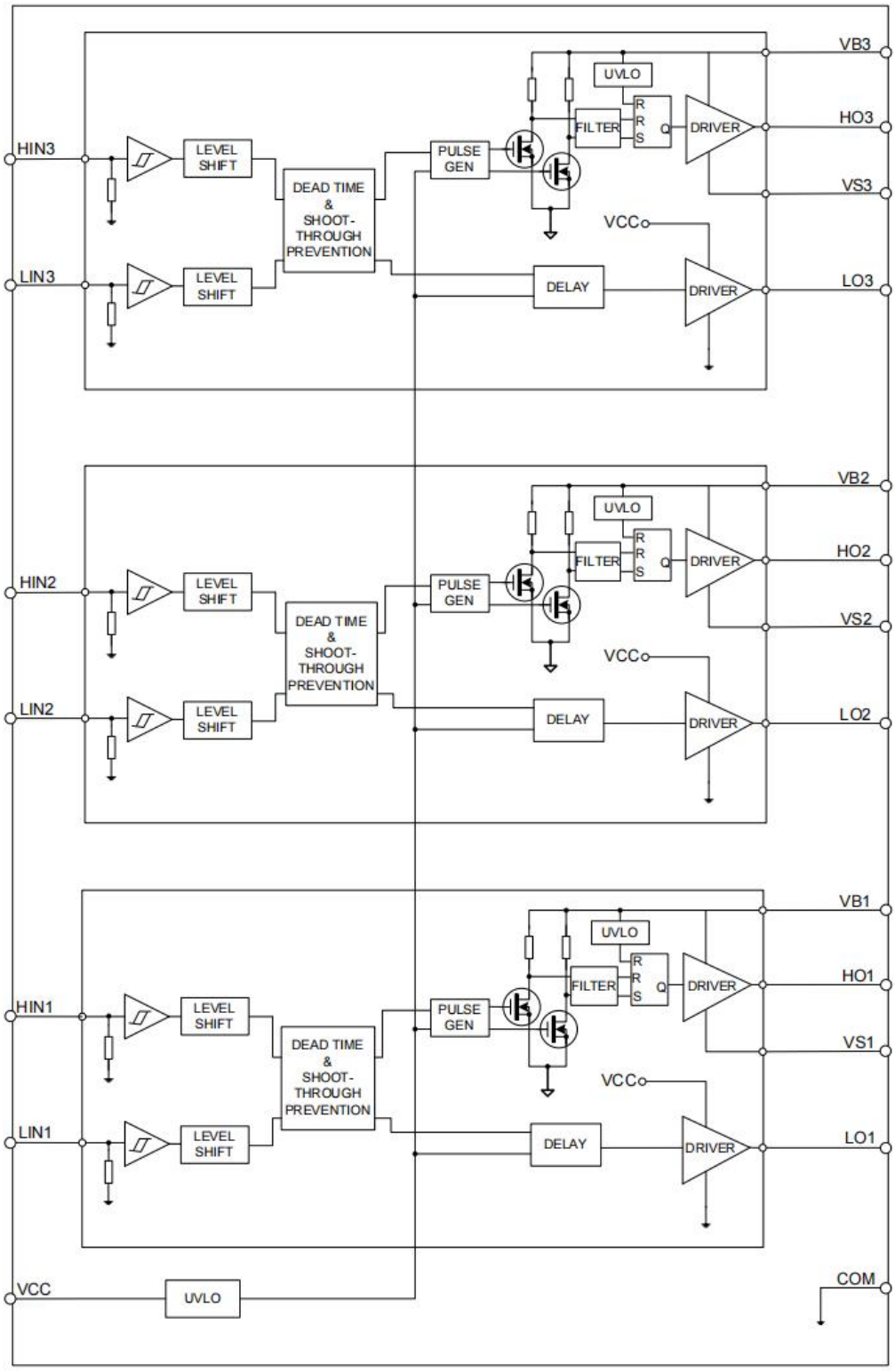
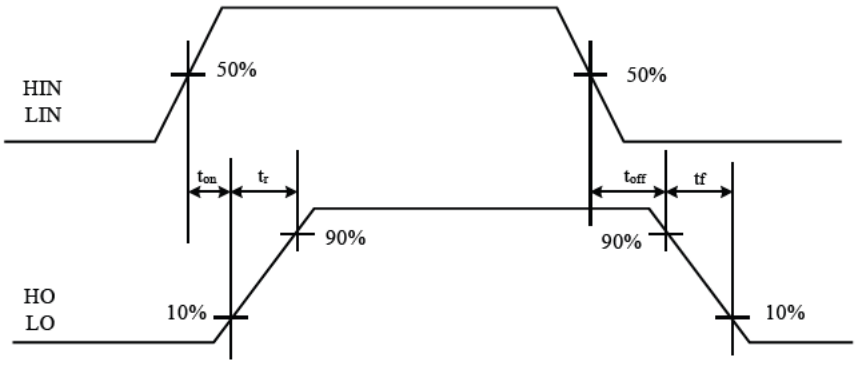
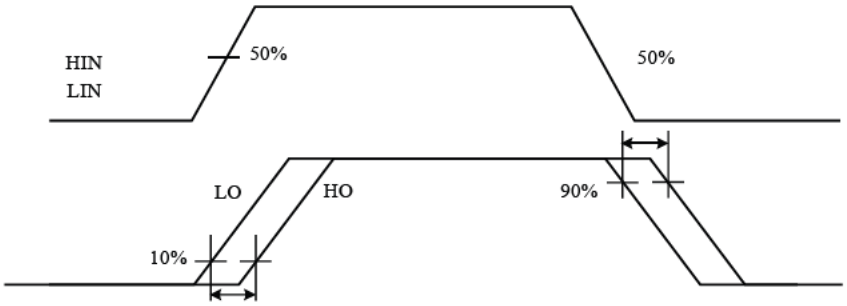


Figure. 2 Functional block diagram of the XJ1801

6.2 Switching Time Waveform Definitions

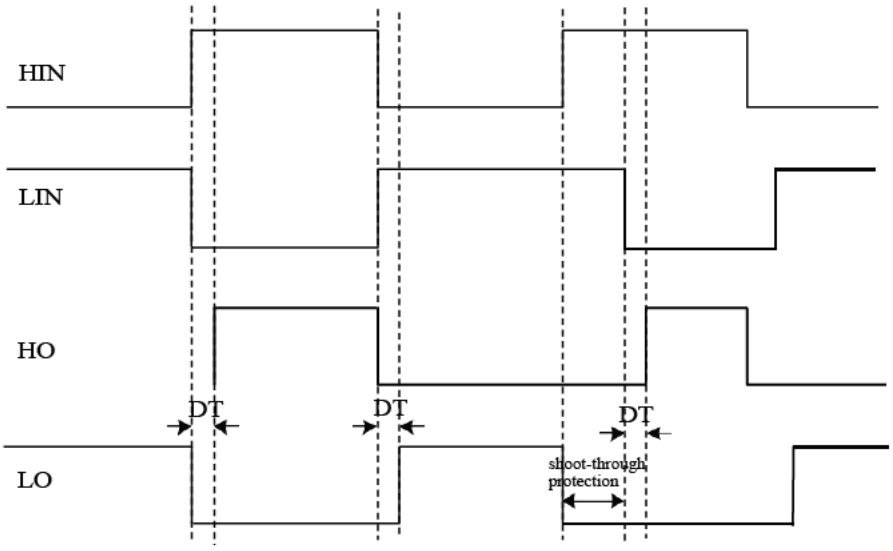


6.3 Delay Matching Waveform Definitions



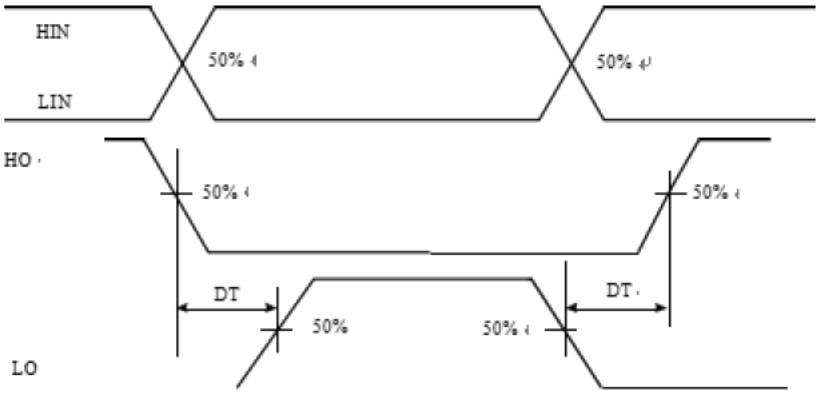
6.4 Input/Output Timing Diagram

The chip is designed with a protection circuit specifically designed to prevent power tube direct current. This design can effectively prevent direct current damage to the power tube caused by interference on the high-side and low-side input signals. The following figure shows how the direct current prevention circuit protects the power tube



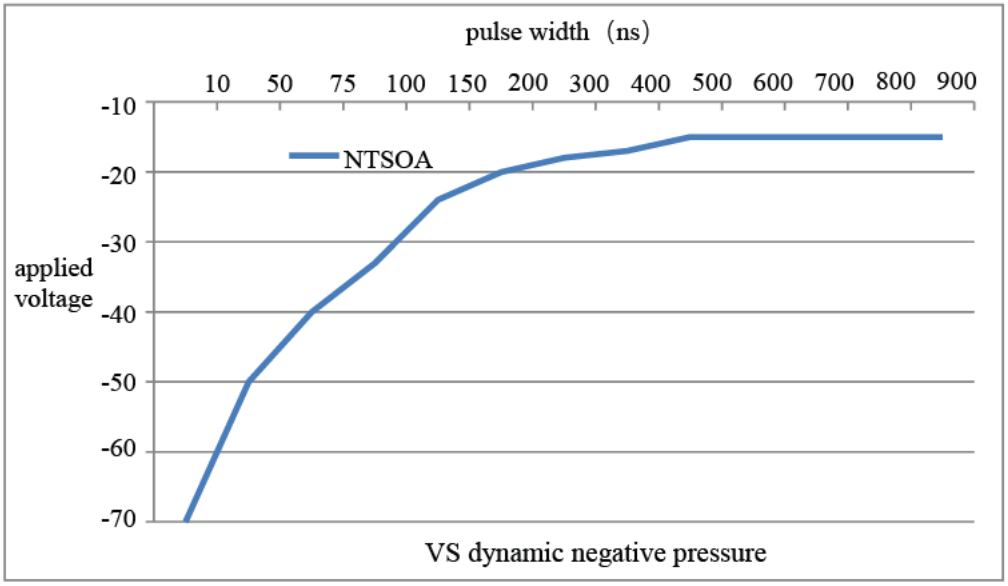
6.5 Deadtime Function

A fixed dead time protection circuit is set inside the chip. During the dead time, both the high-side and low-side outputs are set to a low level. The dead time set must ensure that after one power tube is turned off, another power tube is turned on, so as to effectively prevent the shoot-through phenomenon of the upper and lower power tubes. If the external dead time set by the logic input is greater than the dead time set inside the chip, the external dead time set by the logic input is used as the chip output dead time; if the external dead time set by the logic input is less than the dead time set inside the chip, the dead time of the chip output is the dead time set inside the chip.



6.6 Transient negative voltage safe working area

JSC1801 uses the transient negative voltage safe operating area (NTSOA) to characterize the gate driver's ability to handle transient negative voltages. The gate driver can work properly for any negative pulse whose amplitude and pulse width are above the blue line shown in the figure below. Pulses with excessive amplitude (below the blue line) may cause the gate driver to malfunction.



7 System Applications

The typical application diagram of JSC1801 is shown below:

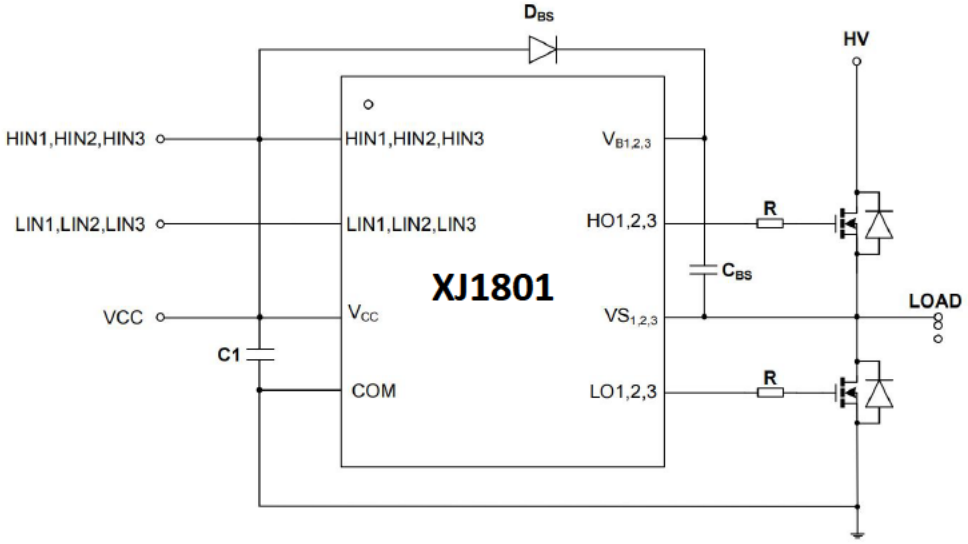


Figure. 3 Typical connection diagram

C1： Power filter capacitor, according to the circuit can choose 1μF ~ 10μF.

R： Gate drive resistor, and the resistance depends on the device being driven and deadtime.

D_{bs}： Bootstrap diodes. the diodes with high reverse breakdown voltage (> 250V) and short recovery time should be selected.

C_{bs}： Bootstrap capacitors. Ceramic capacitors or tantalum capacitors should be selected, the minimum capacitance can be calculated according to the following formula

$$Cbs \geq 15 \cdot \frac{2 \cdot \left[2 \cdot Q_g + Q_{period} + \frac{I_{bs(static)}}{f} + \frac{I_{bs(leak)}}{f}\right]}{V_{CC} - V_F - V_{ds(L)}}$$

Q_g is the gate charge of the high-side power device ;

Q_{period} is the charge requirement of the level conversion circuit in each cycle, which is about 10 nC ;

$I_{bs\,(static)}$ is the static current of the high-side drive circuit;

$I_{bs\,(leak)}$ is the leakage current of bootstrap capacitor;

f is the working frequency of the circuit;

V_{CC} is the low-side supply voltage;

V_F is the forward voltage drop of the bootstrap diode;

$V_{ds\,(L)}$ is the on-state voltage drop of low-side power devices.

Note : The above lines and parameters are for reference only. The actual application circuit sets parameters according to the measured results.

8 Electrical characteristics

8.1 Maximum Absolute Conditions (COM is used as the reference point for all pins unless otherwise specified)

If the maximum absolute condition of the electrical characteristics is violated, the chip may be permanently damaged. Refer to the chip function working limit shown in the following table.

parameter		Symbol	Range	unit
High side floating absolute voltage		$V_{B1,2,3}$	-0.3～250	V
Static high-side floating offset voltage		$V_{S1,2,3}$	$V_{B1,2,3}$-25～$V_{B1,2,3}$+0.3	V
Dynamic high-side floating offset voltage		$V_{HO1,2,3}$	$V_{S1,2,3}$-0.3～$V_{B1,2,3}$+0.3	V
High-side output voltage		V_{CC}	-0.3～25	V
Low-side supply voltage		$V_{LO1,2,3}$	-0.3～V_{CC}+0.3	V
Logic input voltage (HIN, LIN)		V_{IN}	-0.3～V_{CC}+0.3	V
Offset voltage slew rate range		dV_S/dt	≤50	V/ns
Power dissipation@T_A≤25℃	TSSOP20	P_D	≤1.25	W
	QFN24	P_D	≤3.0	W
Thermal resistance of paired environment	TSSOP-20	R_{thJA}	≤100	C/W
	QFN24	R_{thJA}	≤42	C/W
Junction temperature range		T_j	≤150	C
Storage temperature range		T_{stg}	-40～120	C

Table. 2 The maximum absolute conditions of the XJ1801

8.2 Recommended normal working conditions (all voltages are based on COM as reference point)

It is recommended not to exceed the recommended working conditions, or to design the absolute maximum rating as the working conditions.

parameter	Symbol	minimum value	maximum value	unit
High side floating absolute voltage	$V_{B1,2,3}$	$V_{S1,2,3}$+4.9	$V_{S1,2,3}$+20	V
Static high-side floating offset voltage	$V_{S1,2,3}$	COM-2(Note 1)	250	V
Dynamic high-side floating offset voltage	$V_{S1,2,3}$	-50(Note 2)	250	V
High-side output voltage	$V_{HO1,2,3}$	$V_{S1,2,3}$	$V_{B1,2,3}$	V
Low-side supply voltage	V_{CC}	4.9	20	V
Low-side output voltage	$V_{LO1,2,3}$	0	V_{CC}	V
Logic input voltage (HIN, LIN)	V_{IN}	0	V_{CC}	V
Ambient temperature	T_A	-40	125	C

Table. 3 Recommended normal working conditions of the XJ1801

Note 1: When $V_{S1,2,3}$ is (COM-2V) to 250V, HO works normally. When $V_{S1,2,3}$ is (COM-2V) to (COM-V_{BS}), the HO logic state is maintained.

Note 2: VS1,2,3 is (COM-50V), 50ns wide transient negative voltage, HO works normally.

8.3 Input electrical characteristics

a) Static electrical characteristics (unless otherwise specified, TA = 25C, VCC = VBS1,2,3 = 15V, VS = COM)

parameter	Symbol	test condition	value	unit
High level input threshold voltage	V_{IH}		2.7	V
Low level input threshold voltage	V_{IL}		1.3	V
V_{CC} under-voltage protection tripping voltage	V_{CCUV+}		4.7	V
V_{CC} undervoltage protection reset voltage	V_{CCUV-}		4.5	V
V_{CC} undervoltage protection hysteresis voltage	V_{CCUVH}		0.2	V
V_{BS} undervoltage protection tripping voltage	V_{BSUV+}		4.7	V
V_{BS} undervoltage protection reset voltage	V_{BSUV-}		4.5	V
V_{BS} undervoltage protection hysteresis voltage	V_{BSUVH}		0.2	V
Leakage current of suspension power supply	I_{LK}	$V_{B1,2,3}$=$V_{S1,2,3}$=250V	0.3	μA
V_{BS} static current	I_{QBS}	V_{IN}=0V or 5V	160	μA
V_{BS} Dynamic Current	I_{PBS}	$f_{HIN1,2,3}$=20kHz	170	μA
Static current of V_{CC}	I_{QCC}	V_{IN} =0V or 5V	160	uA
V_{CC} dynamic current	I_{PCC}	$f_{LIN1,2,3}$=20kHz	160	uA
LIN high level input bias current	I_{LIN+}	V_{LIN}=5V	25	μA
LIN low level input bias current	I_{LIN-}	V_{LIN}=0V	0.1	μA
HIN high level input bias current	I_{HIN+}	V_{HIN}=5V	25	μA
HIN Low Level Input Bias Current	I_{HIN-}	V_{HIN}=0V	0.1	μA
Input pull-down resistance	R_{IN}		190	KΩ
high level output voltage	V_{OH}	I_O=100mA	0.7	V
low level output voltage	V_{OL}	I_O=100mA	0.3	V
High-level output short-circuit pulse current	I_{OH}	V_O=0V，V_{IN}=5V，PWD≤10μs	0.9	A
Low-level output short-circuit pulse current	I_{OL}	V_O=15V，V_{IN}=0V，PWD≤10μs	1.35	A
V_S static negative pressure	V_{SN}		-6	V

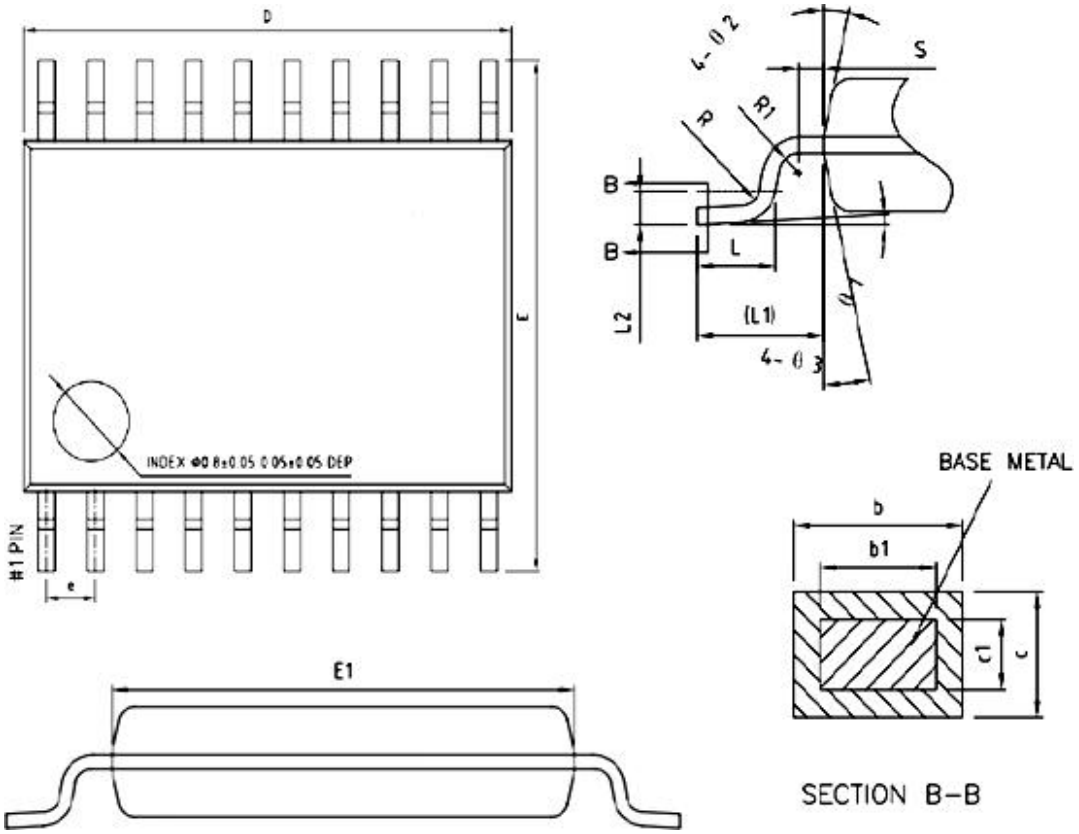
Table. 4 Input electrical characteristics of the XJ1801

b) Dynamic electrical characteristics (unless otherwise specified, T_A = 25℃, V_{CC} = $V_{BS1,2,3}$ = 15V, V_S = COM)

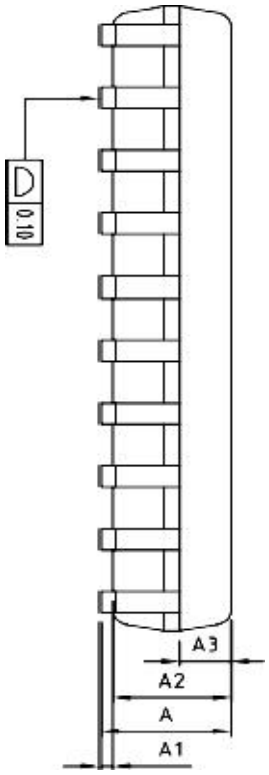
parameter	Symbol	test condition	value	unit
Output rising edge transmission time	ton		350	ns
Output falling edge transmission time	toff		130	ns
Output rise time	t_r	C_L=1000pF	46	ns
Output drop time	t_f	C_L=1000pF	45	ns
High and low side delay matching	MT		--	ns
dead time	DT		250	ns

9 Package size diagram

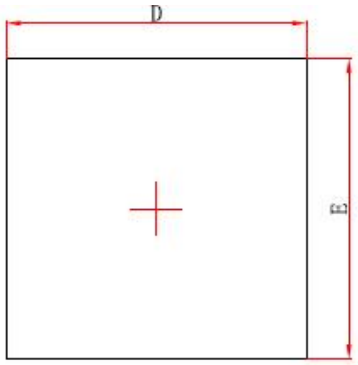
9.1 TSSOP20



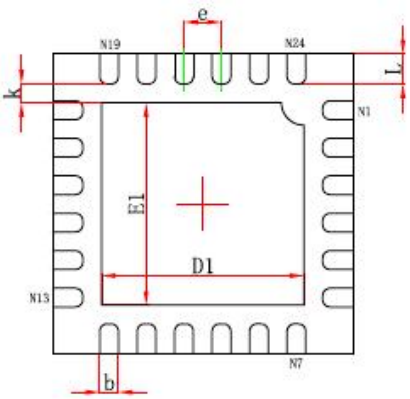
	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.80	1.00	1.05
b	0.19	—	0.30
b1	0.19	0.22	0.25
c	0.09	—	0.20
c1	0.09	—	0.16
D	6.40	6.50	6.60
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00BSC		



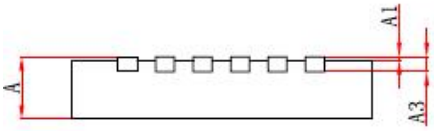
9.2 QFN24



Top View



Bottom View



Side View

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700/0.800	0.800/0.900	0.028/0.031	0.0031/0.0035
A1	0.000	0.050	0.000	0.002
A3	0.203REF		0.008REF	
D	3.924	4.076	0.154	0.160
E	3.924	4.076	0.154	0.160
D1	2.600	2.800	0.102	0.110
E1	2.600	2.800	0.102	0.110
K	0.200MN		0.008MN	
B	0.200	0.300	0.008	0.012
E	0.500TYP		0.020TYP	
L	0.324	0.476	0.013	0.019

10 Software Description

According to the actual use of the control software programming

11 Application development board

The example diagram is a 24 V BLDC motor drive circuit, and the driving MOS tube should be as large as possible. Meet the demand of output large current

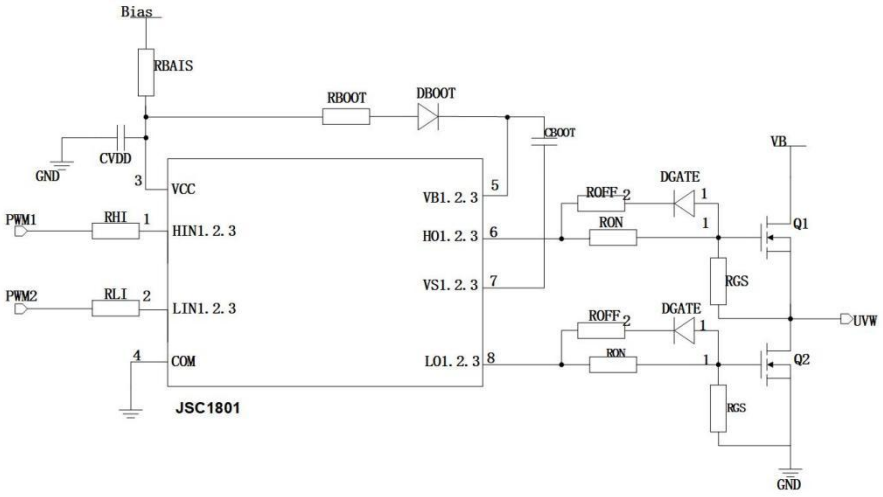


Figure. 4 Application development board