WBC-AIA381-M10

Datasheet

catalogs

1. Product Overview

The WBC-AIA381-M10 is a high signal-to-noise ratio, high acoustic overload point, while integrating an ultra-low-power analog-to-digital hybrid "sense-The module is a smart microphone module with an integrated AI chip, “Storage-Computing”. The module has a built-in MEMS Sensor, ASP intelligent voice simulation preprocessing unit, and NPU processing unit, which can realize ultra-low-power offline human voice detection, keyword recognition and other interactive functions.

1.1. Main characteristics

1.1.1. High performance microphone

- Package Size 3.5 x 2.65 x 1.0mm
- Sensitivity ±1dB
- High signal-to-noise ratio 65dBA
- High Acoustic Overload Point 129dBSPL

1.1.2. Built-in neural network processor (NPU)

- Neural Network Computing BNN/CNN Processor Cores
- Supports ultra-low power voice wake-up
- Supports VAD voice detection

1.1.3. Analog Preprocessing (ASP)

- LNA eight levels of configurable gain
- Automatic GainControl
- Event-driven, ultra-low-power analog-to-digital converters

1.1.4. Built-in human voice detection and keyword recognition

- Built-in μW-level ultra-low power analog VADs
- KWS supports up to 30 keywords

1.1.5. memory (unit)

- Supports 32KB OTP
- Built-in 64KB SRAM

1.1.6. peripheral interface

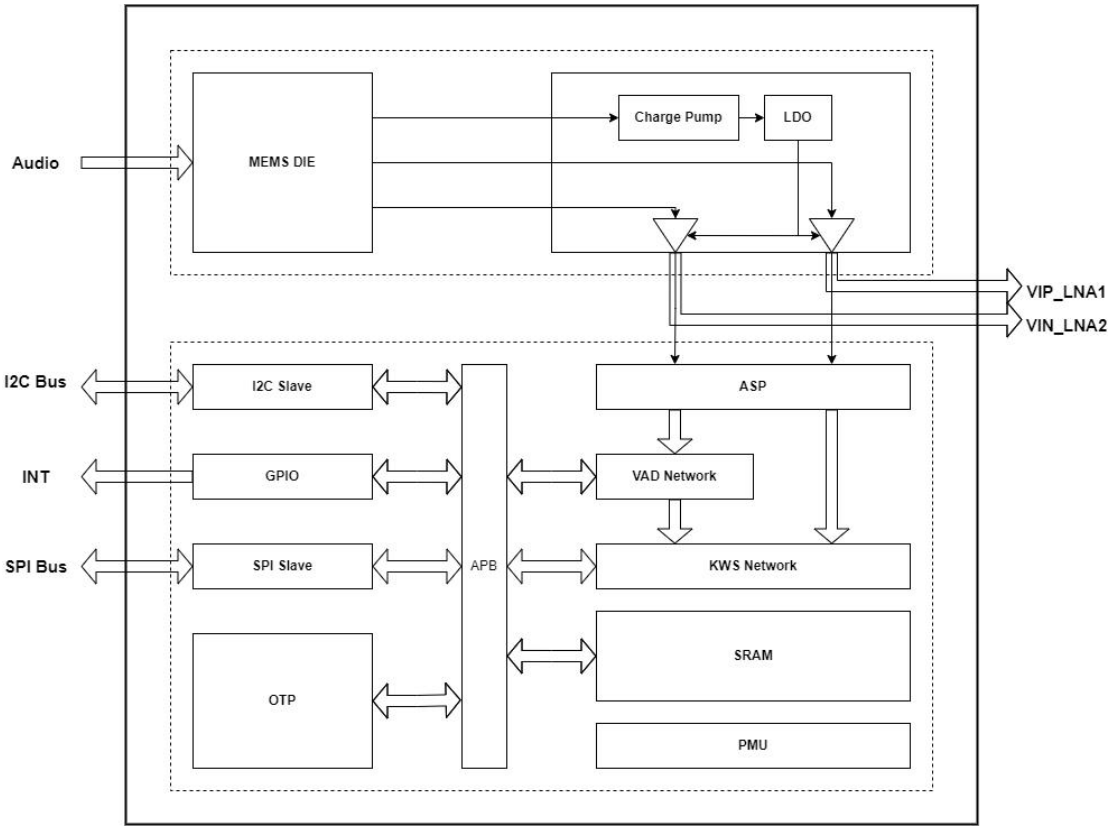
- 1 Slave I2C interface

1.1.7. typical application

- TWS headphones, smartwatches, AR/VR glasses, cell phones, smart homes, etc.

2. Functional Description

2.1. functional block diagram



2.2. Module Function Introduction

- ASP: Analog Signal Processing, an analog signal processing unit that performs signal processing such as filtering and feature extraction on the analog signal of the Microphone.
- LP_NPU: Low-power Neural Processor. This unit is based on the principle of detecting non-stationary signals by small binary BNN neural networks, and performs binary classification of the smooth characteristics of the input signals, which can be used for tasks such as low-power voice detection (VAD, Voice Activity Detection) and anomaly event detection (AED, Anomaly Event Detection), etc. The overall power consumption of LP_NPU is also very low, so it can be kept in the operating state (AON, Always-on). The overall power consumption of LP_NPU is also very low, so it can be always on (AON, Always-on), and only wake up the NPU for more complex neural network classification after detecting a valid voice signal or anomalous event, and also trigger an interrupt output to report to the external master SoC.
- NPU: Neural Processor. The NPU is composed of deep separable CNN networks, which can perform multi-classification on the input data, and can be widely used for keyword spotting (KWS), scene classification, etc. The NPU can trigger an interrupt to report to the external master SoC when it finds the pre-trained classification output. When the NPU discovers the pre-trained classification output, it can trigger an interrupt to report to the external master SoC, which can be configured to sleep by default, waiting for the output of LP_NPU to wake up the NPU.

Wake up and return to hibernation after completing the categorization task.

- PMU: Power Management Unit, which manages the low power consumption of each unit and generates the timing control signal for mode switching. It manages the low power consumption of each unit and generates the timing control signals for mode switching.PMU turns off the NPU by default until the LP_NPU output wakes up other functions; it also turns off the unit after the NPU finishes its task.
- SCR: System Control Register. SCR: System Control Register. It performs the configuration of internal circuits, the communication of peripheral ports, and the management of internal and external interrupts. After power-on, the system starts from the internal OTP, configures the peripheral interface unit parameters, completes the basic configuration of the chip (peripheral port), and waits for the external master chip to configure the internal LP_NPU and NPU parameters through the peripheral port.
- CRG: Clock & Reset Generator. Provides clock and reset signals for each module.
- APB Matrix: Internal APB interconnect bus that connects the HAC to the peripherals and the VAD/KWS units to accomplish data interoperability between the units.
- I2C Interface: I2C standard interface for communication between the chip and external devices.
    - Standard two-wire mode, including data line SDA and clock line SCL
    - Supports up to 400Kb/s
    - Only slave mode is supported
    - Only 7bit addresses are supported
- Supports Burst read and write internal storage

3. operating mode

3.1. Human Voice Recognition Mode (VAD Mode)

In this mode, the chip is always in the state of human voice detection and recognition inference calculation, and the power consumption of the chip is very low about 70uA; when the result of the inference is humanvoice,aninterruptwillbeissuedtowakeupthecontrollerorotherprocessors.Whentheinferenceresultisahumanvoice,an interruptwillbesenttowakeupthecontrollerorotherprocessors.

3.2. Continuous speech recognition mode (KWS mode)

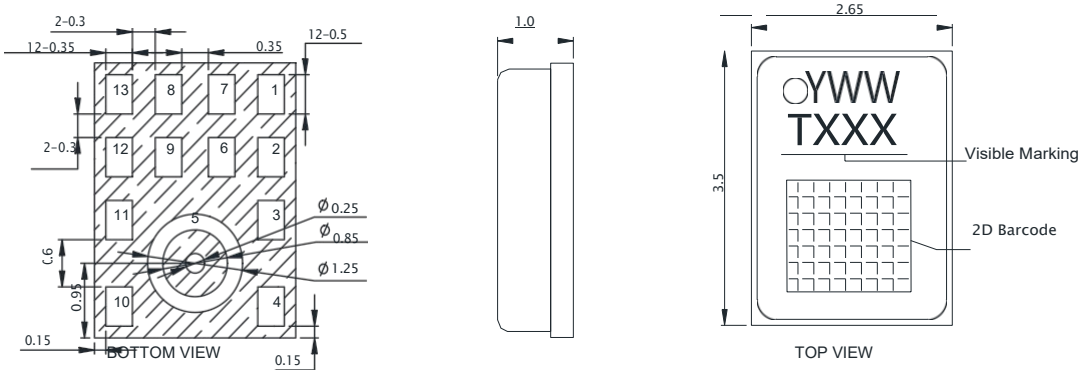
In this mode, the chip has been in the keyword recognition inference calculation, the power consumption has been at about 160uA; after the inference result matches with the pre-trained result successfully, an interrupt will be issued to wake up the controller or other processors; the controller or processor receives the interrupt and reads the keyword result in the specified register through the IIC data port actively to carry out the relevant actions.

3.3. Low power Voice wake-up mode (VAD+KWS mode)

In this mode, the chip is always in the human voice detection and recognition inference calculation, and the power consumption of the chip is very low about 70uA; secondly, when the inference resultis ahumanvoice, the internaltrigger mechanismwillbeactivated to makethechip enter into the KWSmodefor thekeyword recognitioninference calculation. Finally, whenthekeyword inferenceresultmatches thepre-trained resultsuccessfully, aninterruptwillbeissued to wakeup thecontroller or other processors; after receiving the interrupt, the controller or processors will actively read the keyword result in the specified register through the IIC data port.

From there, the relevant actions are performed.

4. machine structure



Unit: mm UnmarkedTolerance: ± 0.1 (mm)

Item	Dimension	Tolerance
Length	3.5	±0.1
Width	2.65	±0.1
Height	1.0	±0.1
Acoustic Port	0.25	±0.05

No	PIN Name	Direction	Description
1	VCC	P	Processor Analog Power Supply
2	VDD	V	Microphone Power Supply
3	PAD_VADINT	DO	VAD Wake-up interrupt output
4	AGND	G	analogically
5	GND	G	middleground
6	PAD_KWSINT	DO	KWS Wake-up interrupt output
7	VIP_LNA1	AOUT	Analog microphone signal output
8	PAD_RSTN	DI	Processor hardware reset port
9	VDDIO	P	Processor Digital IO Power Supply
10	DGND	G	digital land
11	PAD_SDA	DIO	I2C Slave interface data pin
12	PAD_SCL	DI	I2C Slave Interface clock pin
13	DVDD09	AIO	Digital Core Power

5. Electrical Characteristics

5.1. limit parameter

Parameter	Min	Typ	Max.	Unit
Processor Related:				
analog power	-0.3		3.6	V
Digital IO Power Supply	-0.3		3.6	V
VIP_LNA1	-0.3		3.6	V
Other inputs and outputs	-0.3		3.6	V
Microphone related:				
Power Supply Power Supply			4.2	V
System and package related:				
Operating Temperature Range	-40		85	℃
Storage temperature range	-40		100	℃
ESD (HBM)	-2000		2000	V

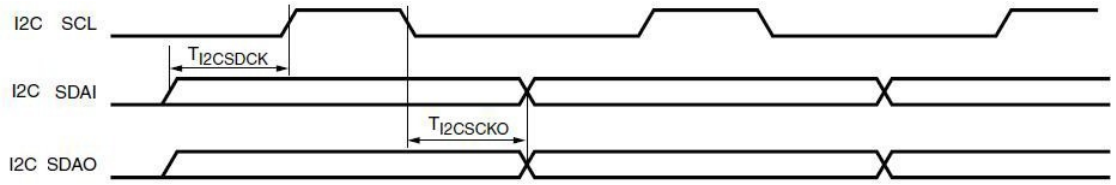
5.2. Performance specifications

Parameter	Symbol	Condition	Min	Typ	Max.	Unit
Processor Related:						
Standby power consumption		VAD is active, KWS is dormant.		70		μA
activation state		Both VAD a n d KWS are operational.		170		μA
VAD Detection Delay		Signal from analog microphone arrives at VAD unit to VAD output interrupt.	2			ms
KWS Detection Delay		From voice finish to KWS unit output interrupt	100			ms
Microphone related:						
power supply	VDD		2.3	2.75	3.6	V
(level of) sensitivity	S	f=1KHz, Pin=1Pa, 0dB=1V/Pa	-39	-38	-37	db
directivity			omnidirectional			
polarities		Sound Pressure Variation Characteristics	Output Voltage Increase			
Sensitivity vs.	ΔS	Vs=3.6V~2.3V		<0.5		dB
Output Impedance	Zout	f=1kHz			400	Ω
Current power consumption	I	1.6 V to 3.6 V	135		200	μA
signal-to-noise ratio	S/N	20-20KHz Bandwidth, A-Weighted		65		dBA
THD	THD	94dB SPL @1KHz		0.05	0.5	%

		125dBSPL @1KHz		1		
Acoustic overload point	AOP	THD 10%@1KHz		129		dBSPL
power supply suppression	PSR	100mVpp Squarewave @217Hz, A-weighted			-90	dB
Power Supply Ripple Rejection Ratio	PSRR	200mVpp Sinewave @1KHz	60			dB
DC Output	VDC			1.10		V
Output Load	Cload				100	pF
	Rload		8			KΩ

5.3. I2C Digital Interface Features

a. I2C Interface Timing



b. I2C Interfac

Descriptio n	Min	Typ	Max .	Unit
TDCI2CFCLK	SCL duty cycle	-	50	-	%
TI2CFCKO	SDAO clock to out delay	-	-	900	ns
TI2CFDCK	SDAI setup time	100	-	-	ns
FI2CFCLK	SCL clock frequency	-	-	400	KHz

6. PCB Design and Layout Guide

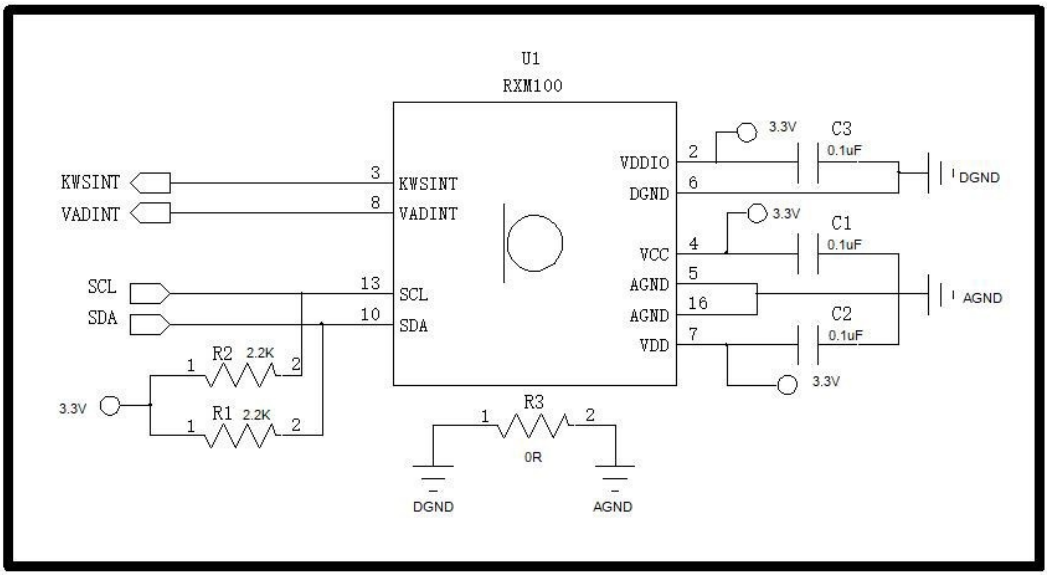
6.1. power layer

Power supply noise has a critical impact on analog circuits, and system power design requires the use of low impedancepowersupplylayersanddecouplingcapacitors. Itisrecommendedthatnoise-sensitivepowersupplypinsmayalso need to be connected to decoupling capacitors (0.1μF), and the shorter the traces, the better, as long traces may couple additional noise into the power supply.

6.2. signal path

- The MIC alignment is as short as possible, the alignment is wrapped around the ground as much as possible, and the bottom reference ground plane is as complete as possible.
- Place the MIC circuit as far away as possible from sources of interference (DCDC inductors, crystals, high current networks, etc.).
- The analog and digital grounds should be separated and eventually shorted with a 0 ohm resistor.
- Power supply filter capacitors are placed as close to the pins as possible.

6.3. typical application



I2C Mode Application Diagram

Introduction to I2C read and write:

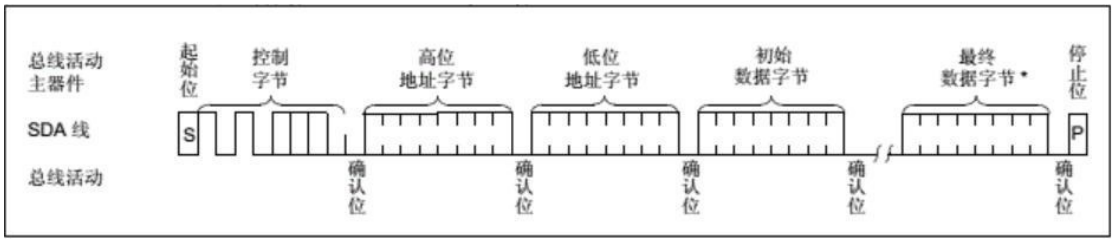
a. The I2C interface slave address of the chip is a 7-bit address at 0x5A.

b. According to the I2C protocol, the read/write bit R is high and W is low.

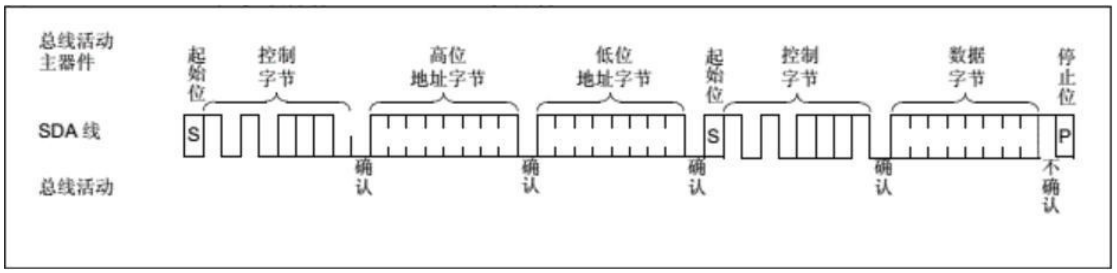
c. Address and data are sent with the high byte first and the low byte second.

d. When the address and data bytes are sent, the MSB is sent first and the LSB is sent second.

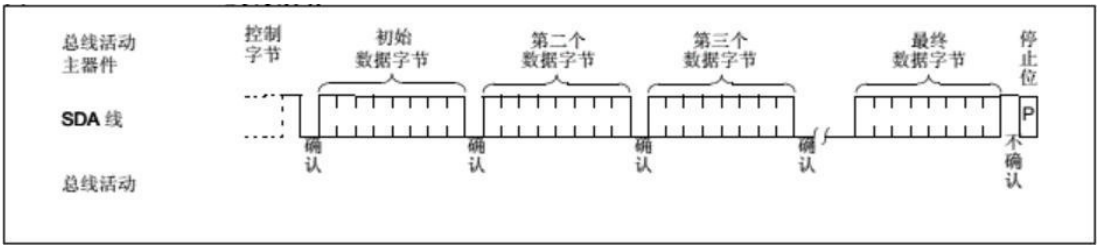
When I2C writes a register, the timing is as shown below:



When I2C reads the registers byte byte, the timing is as shown below.



When I2C sequential byte read registers, the timing is as shown below.



7. Reliability Specifications

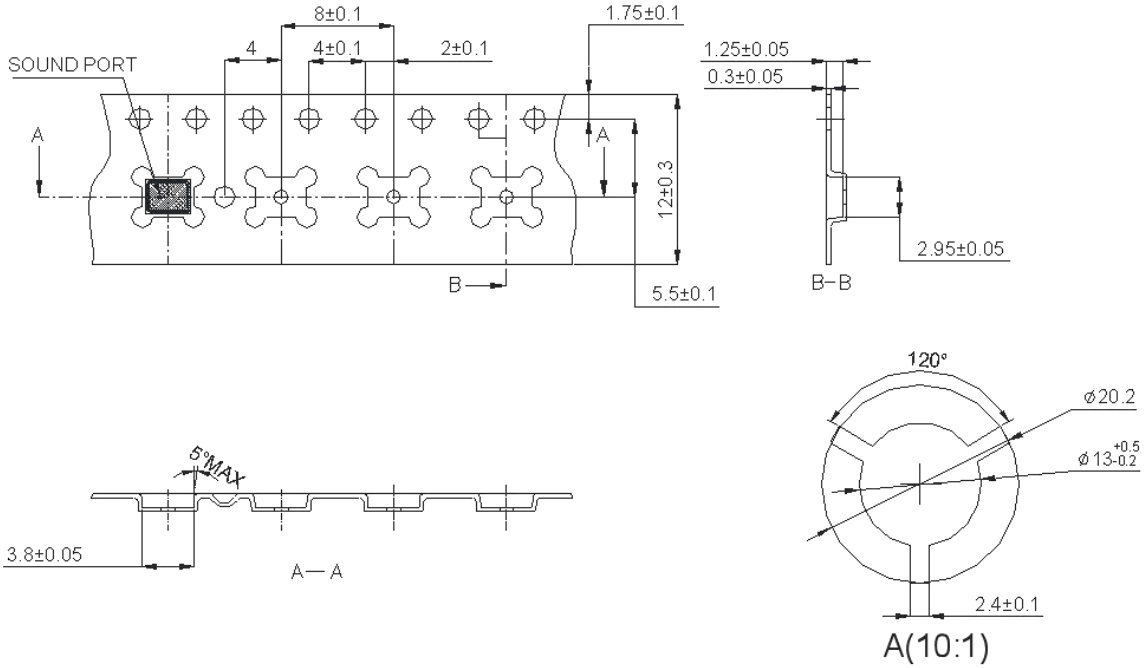
No.	Item	Test condition
1	preprocessing	Baking: 125 degrees/24 hours, immersion 85 degrees 85%RH 168H, complete reflow 3 times, maximum reflow temperature 260 degrees.
2	High temperature storage test	105±3℃, 1000h, 2 hours recovery
3	High temperature power-up test	105±3℃, upper limit voltage, 1000h, recovery 2 hours
4	Low temperature storage test	-40±3℃, 1000h, recovery 2 hours
5	Low temperature power-up test	-40±3℃, upper limit voltage, 1000h, recovery 2 hours
6	High temperature and high humidity power-up test 1	85±3℃, 85%RH, at upper bias voltage, 1000h, recovery 2 Hours, after the test microphone internal should be free of corrosion and deformation
7	High temperature and high humidity power-on test 2	65±3℃, 95%RH, at the upper limit of bias voltage, 168h, recovery 2 hours, after the test microphone internal should be free of corrosion and deformation
8	Temperature shock test	Double-box method, -40℃15min→125℃15min, 100 cycles, recovery 2 hours
9	Vibration test	X, Y, Z directions, 12 minutes each direction, frequency: 20~2000Hz, peak acceleration 20g, recovery 2 hours
10	Drop test	Height: 1.5 meters Fixture weight: 150g (Diameter of the sound hole in the fixture >= 0.8 mm) Reference surface: smooth marble flooring Duration: 4 corners * 4 times, 6 surfaces * 4 times after the test sensitivity change should be less than 1dB
11	Roller test	Height: 1.0 meters Fixture weight: 150g (Diameter of sound hole in fixture >= 0.8mm) Duration: 300 times

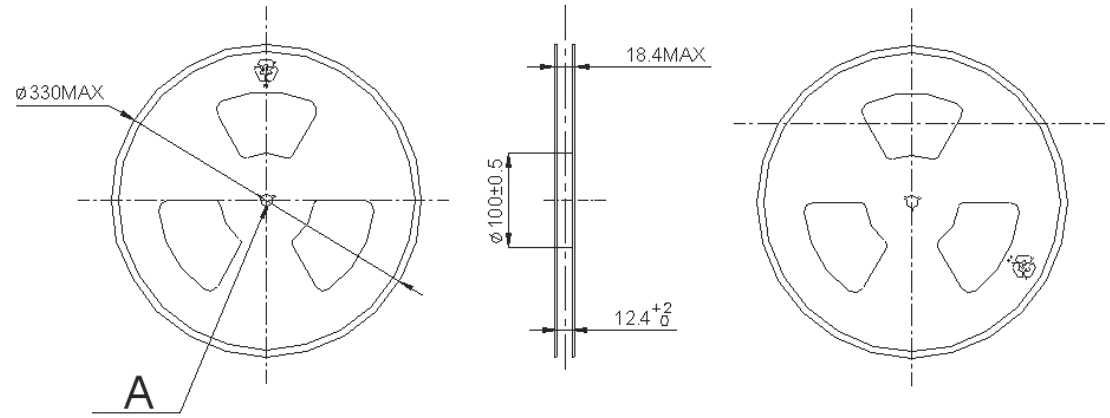
		Recommended frequency: 10-11 times / Min The change in sensitivity after the test should be less than 1dB.
12	Static test 1	a. HMB Discharge position: I/O pin Charge voltage: ±3000V Discharge network: 100pF & 1500Ω b. CDM Discharge position: I/O pin Charge voltage: ±250V
13	Static test 2	The test is carried out in accordance with IEC 61000-4-2 standard level 3: a. contact discharge Discharge position: MIC Charge voltage at output: ±6000V DC dischargenetwork: 150pF & 330Ω b. air discharge Discharge position: sound hole Charge voltage: ±8000VDC Discharge network: 150pF&330Ω
14	Structural impact test	10000 grams, duration: 0.1 ms, X/Y/Z 3 directions, 3 times in each direction, the change of sensitivity should be less than 1dB after the test.
15	circumfluence	According to the reflux profile, 3 refluxes with a peak temperature of +260°C were performed.

8. wrap

* Packaging with anti-static trays and belts....

* Static protection measures should be taken during packaging operations.

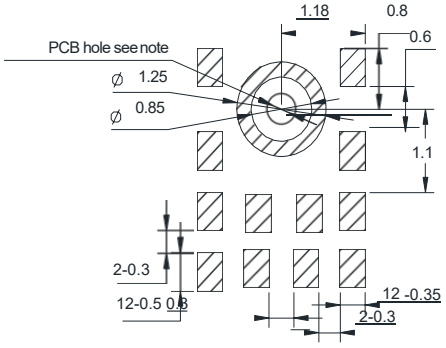




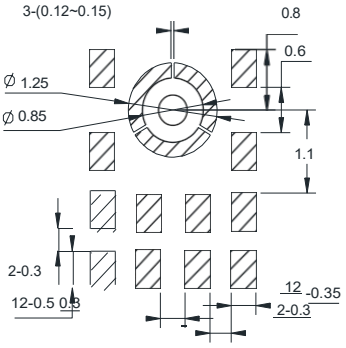
Tape and Reel	ϕ330mm	5,500PCS×1=5,500PCS
Shipping Box	215mm*370mm*370mm	5,500PCS×10=55,000PCS

9. Application Design Recommendations

9.1. Recommended pad design and solder paste printed board design



Recommended PCB pad design



Suggested designfor solder paste printed circuit boards

Caution.

Unless otherwise specified, dimensions are in millimeters.

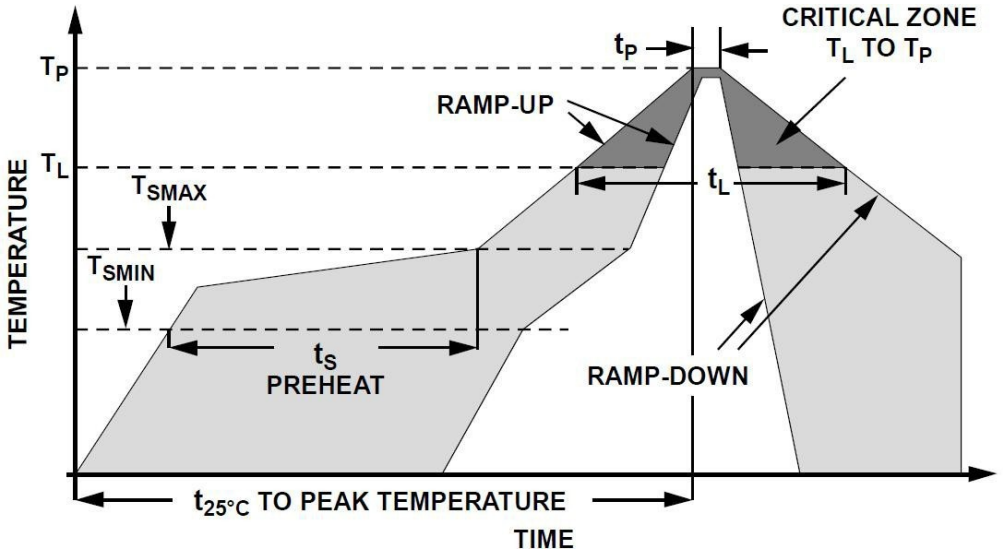
Unless otherwise specified, the tolerance is ±0.1mm.

Recommended PCB non-metallized hole diameter is 0.4-0.6mm.

9.2. Reflow temperature profile

Temperature distribution during reflow

parameters		consultation	standardize
average rate		TL to TP	Up to 3°C/sec
preheating	minimum temperature	TSMIN	150°C
	highest temperature	TSMAX	200°C
	Warming time	tS	60 sec to 180 sec
heating rate		TSMAX to TL	1.25°C/sec
Solder Paste Liquid Retention Time		tL	60 sec to 150 sec
liquefaction temperature		TL	217°C
peak temperature		TP	260°C +0°C/-5°C
Time within +5°C of actual peak temperature		tP	20 sec to 40 sec
Rate of temperature decrease		TP to TSMAX	6°C/sec max
Time from +25°C to maximum temperature			8 min max



Reflow Curve Diagram

Annotation:

If multiple refluxes are required, the MIC should be cooled to room temperature before the next reflux.

No more than 3 reflow cycles are recommended.

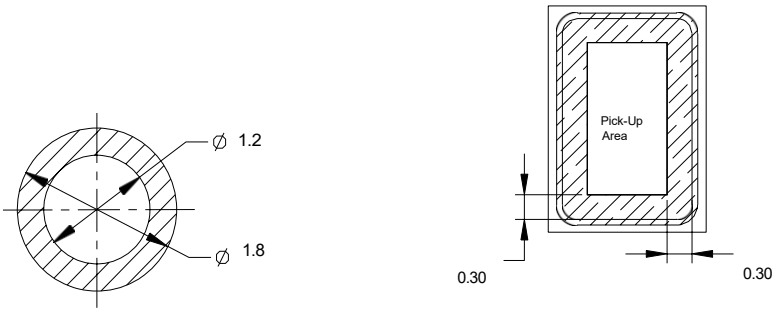
Do not wash the plate with liquid or ultrasound after refluxing. Do not vacuum against the MIC sound hole.

Do not insert any objects into the MIC's sound holes at any time. If double-sided PCBA is used, it is recommended that the MIC be attached during the second pass. do not seal the tone holes during reflow.

If there is a risk of open seams, it is recommended that the peak reflow temperature be set to below 240°C or above 255°C.

9.3. Recommended MIC Nozzles

Outer diameter Φ1.8mm Inner diameter Φ1.2mm



Nozzle size and MIC suction area

10. Special Notes

10.1 Airsoft Cleaning Specifications

Do not point the air gun directly at the MIC sound hole. Recommended Conditions.
Air pressure < 0.3MPa;
distance > 5cm;

Time <5sec.

10.2 wrap

The MIC cannot be stored in a vacuum environment. Vacuum sealing may cause damage to the MIC.

10.3 stockpile

Meets the requirements of MSL (Moisture Sensitivity Level) 1. Store the MIC in a warehouse where the humidity is less than 75% and not in the presence of sudden temperature changes, acidic and any other harmful gases, or strong magnetic fields.
Pleaseprotecttheproductfrommoisture,vibration,light,externalforceand otherfactors. Please take appropriate anti-static measures during assembly and transportation.

Please use the shipping package form for long term storage.

10.4 invalidate

FordiscardedmicrophonesCcustomersshouldcomplywiththeWasteElectricalandElectronicEquipment(WEEE) Directive(2002/96/EC)

11. releases

releases	descriptive	dates
V1.0	first edition	2025-01-14